

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10056373	FILING DATE 01/17/2002	CLASS 250	SUBCLASS 2142	GAU 2878	EXAMINER R. E. S. C.
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**APPLICANTS: Bretschneider Ernst; Fuhrmann Johann; Einfeldt Walter;

**CONTINUING DATA VERIFIED:

None TO BEST AVAILABLE COPY

** FOREIGN APPLICATIONS VERIFIED:

GERMANY 10101995.5 01/18/2001 TMR

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no

ATTORNEY DOCKET NO

DE 010005

Verified and Acknowledged Examiners's initials

TITLE : Circuit arrangement and method of protecting at least a chip arrangement from manipulation and/or abuse

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED

Assistant Examiner

ISSUE FEE

Amount Due Date Paid

Primary Examiner

PREPARED FOR ISSUE

Application Examiner

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FILED WITH: ☐ DISK (CRF) ☐ CD-ROM

CLAIMS ALLOWED

Total Claims Print Claim for O.G.

DRAWING

Sheets Drwg. Figs. Drwg. Print Fig.

CD-ROM

(Attached in pocket on right inside flap)